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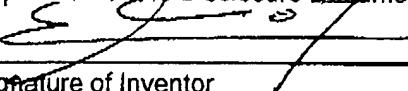
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Title of Invention: Mechanism to activate a context when no stream is running in a multi-streaming processing core

Enclosed is a disclosure of the above-titled invention consisting of 4 sheets of description and 0 sheets of drawings. A check or money order in the amount of 10.00 is enclosed to cover the fee (37 CFR 1.21(c)).

The undersigned, being a named inventor of the disclosed invention, requests that the enclosed papers be accepted under the Disclosure Document Program, and that they be preserved for a period of two years.


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To fill out the form correctly, follow each set of instructions provided with each heading.

Title of Invention

This section is simply a brief descriptive title of the invention.

Insert title here: Mechanism to activate a context when no stream is running in a multi-streaming processing core

Inventors

We will need the residence address, mailing address, full legal names and citizenship of each inventor at the time of submission of the disclosure.

Enrique Musoll

Mario Nemirovsky

Stephen Melvin

Related inventions known or authored by you or your company

This section should list any prior patents known to you or patents that you have already filed if the present invention depends on them for successful practice.

[1] PA3818

Background

This section is used to describe “the state of the art” before being improved or enhanced with your invention. It should include a brief summarization of existing technologies if any that the present invention improves upon or replaces, a description of any specific problems with “the way the art is practiced now”, and a very brief statement of what is needed to improve or replace the existing art. Include references by U.S. patent number any closely related patents discovered during any prior-art searches

Begin Background here:

The processing core (SPU) of XCaliber contains several contexts or register files. Whenever the thread being executed in one of the contexts finishes, the context no longer belongs to the SPU, but to the PMU.

A context that is not running any thread will not be able to take any interrupt that might have been generated. Therefore, if all the contexts belong to the PMU, an interrupt that gets generated will not be taken until one of the contexts is again SPU-owned and an stream runs on it.

Thus, a mechanism is needed so that, when all the contexts become PMU-owned, one of the contexts is sent back to the SPU, so that any pending interrupts can be taken and the appropriate interrupt service routine invoked.

This mechanism is described in [1], but there are no claims that cover it.

Description of Invention

This section should explain the basic apparatus and method of practicing your invention according to a preferred state. If certain **apparatus** of the invention is not known in the prior art then indicate so. If a **method** of the present invention is not known in prior art then indicate so. If certain methods and apparatus are known in prior art then they do not have to be greatly detailed. However any new subject matter novel over the prior art should be fully explained and represented by drawings and/or sketches.

Begin description here:

The processing core (SPU) of XCaliber contains several contexts or register files. Whenever the thread being executed in one of the contexts finishes, the context no longer belongs to the SPU, but to the PMU; the stream that finishes executes the RELEASE instruction, and at that time the context becomes PMU-owned. Thus, a context is either PMU or SPU owned.

A context that is PMU owned does not run any thread. Since interrupts will only be taken (i.e. the associate interrupt service routine will be executed) only if an stream is running in a context, then an interrupt that is generated by any entity will not be taken right away if all the contexts belong to the PMU. As soon as one context becomes SPU-owned (and it has the interrupt masked), the interrupt will be taken.

This presents the problem that it may take a long time to start executing the interrupt service routine for an interrupt. The problem is even worse if the interrupt has been generated due to a high priority event that needs immediate processing.

Thus, a mechanism is needed so that either:

- *All the time there is at least one SPU-owned context, or*
- *The amount of time that the SPU has no context owned is very small.*

The first solution is the optimum if the response time to take an interrupt is the primary concern. However, the hardware would need to keep the state of the contexts and not issue any RELEASE instruction for the last stream that finishes. The second solution is simpler to implement, but presents larger latency in the interrupt to be taken.

The solution implemented in XCaliber is the second one, and the mechanism is as follows: whenever all the contexts become PMU-owned, the PMU selects one (any one) and releases it back to the SPU. Moreover, the PMU provides a PC address from which the SPU will start fetching instructions. Optionally this PC address could be fixed within the SPU. The purpose of the thread starting at this PC address is to execute at least one instruction so that any pending interrupt can be taken (if it is masked).

Please have all inventors sign the disclosure and mail a hard copy to CCPA for participation in the document disclosure program. Also e-mail to Mark Boys
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Your cooperation in the filling and return of this form will expedite the processing of your application and increase our chances of obtaining a patent for your invention.

Mark Boys, CCPA